Remarks/Arguments

There are no amendments to the specification or the drawings herein.

In the claims, Claims 1-24 remain and are pending in the application. Claims 6-15 are allowed. Claims 1-4, 16, 20 and 23 are rejected and Claims 5, 17-19, 21, 22 and 24 are objected to. Claims 1 and 5 are amended herein. Reconsideration is respectfully requested.

Applicant amended Claims 1 and 5 above to correct informalities and to better represent subject matter claimed therein. Specifically, Claim 1 is amended to replace "means for generating" with "a generator circuit that generates". Claim 1 is further amended to make it clear that a selectable magnitude of a bias voltage takes on one of, "a plurality of values different from a magnitude of the logic high signal", and to correct an informality noted by the Examiner. Support for the amendment is found in at least Claims 1 and 22, as originally filed, as well as Applicant's specification at Page 5, lines 16-18. Claim 5 is amended to better agree with amended Claim 1. The amendments of Claims 1 and 5 do not narrow the scope of the claims relative to the claims as originally filed and are not being made to overcome any known prior art. No new matter is added. Entry and consideration of the amendments are respectfully requested.

The Examiner objected to Claims 1-5 because of an informality. Specifically, the Examiner suggested that the word "of" be inserted between "an output" and "the PWWTM bias generator". Applicant's amendment of Claim 1 above includes insertion of the word "of" per the Examiner's suggestion. Withdrawal of the objection is respectfully requested.

The Examiner rejected Claims 1-4, 16, 20 and 23 under 35 U.S.C. 102(e) as being anticipated by Vangal, U.S. Patent No. 6,735,131 (hereinafter 'Vangal'). With respect to Claims 1-4 the Examiner contended, "Vangal discloses a programmable weak write test mode bias generator ... having all the elements as recited in claims 1-4". Specifically, the Examiner contended that Vangal disclosed, "means for generating an output signal (#32", Fig. 1, column 1, lines 19-20) at an output the [*sic*] PWWTM bias generator, the signal being a logic high in a default mode (normal mode, column 1, lines 19-20), and the output signal being a bias voltage having a selectable magnitude when in a WWTM (column 1, lines 34-35)". The Examiner

further contended that Vangal discloses, "a set of selection inputs (en0, en1, en2, Fig. 2)" and "the default mode logic high signal being actively maintained when the PWWTM bias generator output is connected to a load (driver 10, Fig. 1)". Without evidentiary support of record, the Examiner contended that, "[t]he bias voltage generated from a current, a mode select input to select the WWTM or the default mode ... are inherent". With respect to Claims 16, 20 and 23, the Examiner further contended that Vangal discloses, "an SRAM array having a weak write pull-down transistor (40, Fig. 1) and a write driver (10, fig. 1); means for biasing the week [*sic*] write pull-down transistor with a bias voltage (#32, Fig. 1 and column 1, lines 19-20) the bias voltage having a voltage equivalent to a logic high level of the SRAM in a default mode (normal mode, column 1, lines 19-20) when WWTM is not active, the bias voltage having a selectable magnitude when in [*sic*] the WWTM is active (column 1, lines 34-35)".

The Examiner equated "#32" in FIG. 1 (e.g., a weak write control signal weak #32) of Vangal with an "output signal" of a PWWTM bias generator and with "means for biasing", as claimed by Applicant in Claims 1 and 16. The Examiner apparently further equated a selectable magnitude of a bias voltage of the output signal claimed by Applicant with stacking of multiple diodes to obtain different weak write current values at an output of a driver 10, according to Vangal. In addition, the Examiner alleged that device 40 disclosed by Vangal is a weak write pull-down transistor.

Applicant respectfully traverses the rejection of Claims 1-4, 16, 20 and 23 in view of Vangal on the grounds that that the Examiner failed to establish a *prima facie* case of anticipation with respect to Vangal. In particular, the Examiner has failed to establish that Vangal disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)) and has also failed to show that Vangal disclose the claimed elements "arranged as in the claim" (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)), both of which are required by the Federal Circuit for establishing and supporting *prima facie* anticipation under 35 U.S.C. 102. In addition, the Examiner has respectfully mischaracterized, misunderstood, and misapplied the disclosure and circuits of Vangal in rejecting Applicant's claims.

Specifically, with respect to at least base Claim 1, Vangal fails to disclose either of, "a bias generator for weak write test mode (WWTM) testing" or "the output signal being a logic high signal in a default mode, and the output signal being a bias voltage having a selectable magnitude when in a WWTM", as recited in Claim 1 before amendment, contrary to the Examiner's contention. As amended herein, Vangal fails to disclose that the bias generator comprises, "a generator circuit that generates an output signal at an output" of the bias generator, as recited therein. Vangal also fails to disclose, "the selectable magnitude taking on a selectable one of a plurality of values different from a magnitude of the logic high signal", as is further recited in amended Claim 1.

Regarding base Claim 16, Vangal fails to disclose, "means for biasing the weak write pull-down transistor with a bias voltage", and further does not disclose either that the bias voltage has, "a voltage equivalent to a logic high level of the SRAM in a default mode when the WWTM is not active" or "the bias voltage having a selectable magnitude when the WWTM is active", as recited therein, contrary to the Examiner's contention. Regarding base Claim 20, Vangal does not disclose either, "generating a bias voltage and applying the generated bias voltage to a gate of a weak write pull-down transistor of a write driver while conducting a WWTM test of the SRAM", or "generating a logic high output signal and applying the logic high output signal to the gate of the weak write pull-down transistor while in a default mode when not conducting the WWTM test of the SRAM", as recited therein, contrary to the Examiner's contention.

Instead, with respect to Fig. 1, Vangal discloses, "an SRAM column write driver 10" of the "prior art" that uses, "conventional inverters 16, 18 (comprised of devices 20, 22, 26, 28)" (Vangal, Col. 1, lines 15-17). The conventional inverter 16 inverts an "input signal din 24" to produce an output signal "bit #12" while the conventional inverter 18 inverts an "input signal din #30" to produce an output signal "bit 14" (Vangal, Col. 1, lines 17-19). At Col. 1, lines 19-20, relied upon by the Examiner, Vangal discloses, "[i]n normal operation, a weak write ***control signal*** weak #32 is held high (logic 1)" (***emphasis*** added). Vangal further discloses that in normal operation, "n-device 40 is also kept on" by the weak #32 control signal being held high (logic 1). As illustrated in FIG. 1 of Vangal, the control signal weak #32 (illustrated as "Weak#" and identified as signal "32") is applied to a gate of n-device

40 having a drain and source connected between "inverters 16, 18" and voltage source "Vss".

Further according to Vangal, "[d]river 10 ***is placed*** into WWTM mode by driving weak #32 low" [i.e., logic 0] (***emphasis*** added), and as a result, "[d]evice 40 also turns off" (Vangal, Col. 1, lines 23-25). In WWTM mode, a "[d]iode connected transistor 44 ... supplies a weak write current onto either bit 12 or bit #14", according to Vangal (Vangal, Col. 1, lines 25-26). The diode-connected transistor 44 is illustrated in FIG. 1 of Vangal as being connected in parallel with n-device 40 between the inverters 16, 18, and "Vss". A gate of the diode-connected transistor 44 is connected to a drain of the transistor 44 and is not otherwise available. "The diode-connected transistor 44 is carefully sized using SPICE simulations" (Vangal, Col. 1, lines 30-31), during a design of the driver 10 and "[m]ultiple diodes can be stacked to obtain different current values" (Vangal, Col. 1, lines 34-35), thereby to establish the size of transistor 44 during design and before fabrication.

The control signal "weak #32" is essentially a mode select signal (i.e., input signal) that switches the driver 10 from a normal or default mode to a weak write test mode (i.e., WWTM), according to Vangal, and is not "an output signal", as claimed by Applicant, contrary to the Examiner's characterization thereof. In particular, when the "weak #32" is high or logic 1, the driver 10 operates in normal mode while "driving weak #32 low" places the driver 10 in WWTM (Vangal, Col. 1, line 20 and line 23). Vangal does not identify a source or means for generating the control signal weak #32.

Furthermore, 'device 40' disclosed by Vangal clearly functions as a bypass transistor to enable/disable an action of the weak-write pull-down transistor in WWTM mode and is not "a weak write pull-down transistor", as contended by the Examiner. In particular, the control signal weak #32 is applied to a gate of device 40 to respectively turn device 40 on and off (see Vangal, FIG. 1 and FIG. 2). As such, device 40, according to Vangal, is ***not*** and cannot be a weak write pull-down transistor. Instead, the weak write pull-down transistor of driver 10, illustrated in FIG. 1 of Vangal, is clearly the "diode-connected transistor 44" disclosed by Vangal. According to Vangal, the diode-connected transistor 44 is bypassed by device 40 in normal operation and sets the level of the weak current produced by the driver 10 when in WWTM mode (See Vangal, Col. 1, lines19-35). Other diode-connected

transistors (i.e., transistors 52, 54, and 56) serve a similar function in the driver 10 when enabled by activating one or more of the n-devices 58, 60, and 62.

Specifically, "a programmable weak current circuit 50", illustrated in Fig. 2 of Vangal, replaces the diode-connected transistor 44 of the prior art driver 10 to produce the write driver, according to Vangal (Vangal, Col. 1, lines 41-42). The circuit 50 makes it, "possible to tune the magnitude of the weak current after fabrication on a chip in order to accommodate fabrication variations" thereby making, "it unnecessary to rely on a weak current element that has a fixed (sometimes inappropriate) size [of the transistor 44] determined in advance by a circuit simulation" (Vangal, Col. 1, lines 43-48). Vangal discloses, "Circuit 50 includes multiple ... parallel diode-connected transistors legs 52, 54, 56" (Vangal, Col., lines 49-50).

Importantly, while the diode-connected transistors 44, 52, 54 and 56 act as weak write pull-down transistors, Vangal does not and respectfully cannot teach or suggest that the diode-connected transistors 44, 52, 54 and 56 have a gate input or may be biased with a bias voltage from a bias generator. Specifically, the gates of transistor 44 and each of the other diode-connected transistors 52, 54 and 56 are connected only to a drain thereof rendering it a "diode-connected" transistor (See Vangal, FIG. 1, "44"). As such, the gate(s) is(are) not available for connection to an output signal of a bias generator.

Additionally, Vangal discloses that enable signals en0, en1, and en2 are used to individually select and enable the legs 52, 54, 56 by controlling respective ones "of three n-devices 58, 60, 62" of the legs. The parallel diode-connected transistors of the legs 52, 54, 56 have nominally different sizes such that proper selection using the enable signals en0, en1, and en2 allows control of the weak current produced. See Vangal, at Col. 1, lines 52-56, "[b]y sizing (weighting) the three diode-connected transistor 52, 54, 56 in the ratio of 1:2:4 and by controlling the binary enable signals en0, en1, and en2 appropriately, seven different levels of weak current can be achieved". This discussion by Vangal serves to further emphasize the role of the diode-connected transistors 52, 54 and 56 as weak write pull-down transistors as well as establishing that enable signals en0, en1, and en2 are associated with enabling these transistors and ***nothing more***.

Consequently, contrary to that contended by the Examiner, Vangal does not disclose "a programmable weak write test mode bias generator", but instead clearly discloses an SRAM cell write driver (i.e., driver 10) that provides control of a produced weak current by way of binary enable signals en0, en1 and en2. The binary enable signal en0, en1 and en2 control the weak current produced by the driver 10 by selecting one or more of a set of parallel diode-connected transistors (i.e., weak write pull-down transistors) that directly establish the achieved weak current level produced by the driver. Moreover, the weak write pull-down transistors are disclosed as "diode-connected transistors" that, by definition, have no gate input or other means of accepting and responding to an applied gate bias voltage from outside the driver 10. Thus, in addition to not disclosing a bias generator, according to Vangal, the driver 10 does not even provide a way to receive and use 'a bias output' from 'a programmable weak write test mode bias generator' even if arguably one were to be added to the driver 10 disclosed by Vangal.

Specifically regarding Claim 1, in addition to not disclosing "a bias generator", the "#32" in FIG. 1 (i.e., weak #32 control signal) is clearly not an ***output signal***, contrary to the Examiner's contention. Instead, the control signal weak #32 is an input signal that is used to select between normal mode and WWTM by turning device 40 on and off, according to Vangal. While weak #32 may be logic high when in normal mode, clearly it is the logic high level of the control signal weak #32 that places the driver 10 in normal mode and not the driver 10 that produces weak #32 with logic high when in normal mode. Thus, the signal weak #32 is not and respectfully cannot be an ***output signal*** of a bias generator, as contended by the Examiner.

Furthermore, Vangal fails to disclose that weak #32 control signal is "logic high in a default [or normal] mode" and that it has or may have, "a selectable magnitude when in a WWTM", as recited in Claim 1. In particular, according to Vangal, weak #32 is clearly a digital signal that is either high (i.e., logic 1) or low corresponding to a normal mode and a WWTM mode, respectively. Nowhere does Vangal disclose or suggest that weak #32 takes on any other values other than high and low. Applicant has amended Claim 1 above to emphasize that the selectable magnitudes of the output signal are more than just logic high and logic low.

Specifically, Vangal does not disclose, "a bias voltage having a selectable magnitude when in a WWTM" at Col. 1, lines 34-35, contrary to the Examiner's contention. Instead, at Col. 1, lines 34-35, Vangal discloses, "[m]ultiple diodes can be stacked to obtain different current values". The stacking diodes is with reference to stacking of multiple diode-connected transistors (e.g., establishing a relative size of the diode-connected transistor) and has nothing to do with a selectable magnitude of a signal (e.g., a bias generator output signal) other than the a signal represented by the weak current supplied by the driver 10 to the SRAM memory cell via the bit lines (i.e., "bit#" and "bit") when in WWTM mode, according to Vangal.

The Examiner's contention with respect to "a set of selection inputs (en0, en1, en2, Fig. 2)" is respectfully irrelevant with respect to the control signal weak #32. In particular, the selection inputs en0, en1 and en2, are unrelated to a level or magnitude of weak #32, according to Vangal. The selection inputs en0, en1 and en2 control a strength of a weak write pull-down function of circuit 50 and effect only a strength of the weak current produced by the driver 10 of FIG. 2 when weak #32 is logic low and the driver 10 is in WWTM mode. Thus, the selection inputs, according to Vangal, are not and cannot be, "a set of selection inputs that control the selectable magnitude of the generated bias voltage in WWTM", as recited in Applicant's Claim 3, contrary to the Examiner's contention.

Similarly, the diode-connected transistors or weak write pull-down transistors of Vangal cannot be biased by a bias voltage. No gate is available in devices 44, 52, 54 and 56 to accept a bias voltage. Thus, Vangal respectfully cannot disclose, "the generated output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM", as recited in Applicant's Claim 2.

Regarding base Claim 16, the control signal weak #32, according to Vangal, is not connected or applied to the weak write pull-down transistor (e.g., diode-connected transistor 44, 52, 54 or 56) but is applied to a gate of a mode select transistor (i.e., device 40). Thus, contrary to the Examiner's contention, weak #32 is not and cannot be the, "means for biasing the weak write pull-down transistor with a bias voltage", recited in Applicant's Claim 16. Furthermore, as discussed above, Vangal fails to disclose that weak #32 has or may have "a selectable magnitude when the WWTM is active", as is further recited in Claim 16. For that matter, the diode-connected transistors 44, 52, 54 and 56 of Vangal are incapable of accepting and being biased by

a bias voltage having a selectable magnitude, as defined and claimed by Applicant, thereby obviating any reason for having a means for biasing the weak write pull-down transistor, according to Vangal.

Regarding Claim 20, the diode-connected transistors 44, 52, 54 and 56 (i.e., weak write pull-down transistors) disclosed by Vangal do not provide a gate connection for applying a bias voltage thereto. As such, Vangal respectfully cannot disclose, "generating a bias voltage and applying the generated bias voltage to a gate of a weak write pull-down transistor", as recited in Applicant's Claim 20, since there is no gate to which the generated bias voltage may be applied. Similarly, the lack of an available gate obviates disclosure of, "generating a logic high output signal and applying the logic high output signal to the gate of the weak write pull-down transistor while in a default mode when not conducting the WWTM test of the SRAM", as further recited in Claim 20. In fact, it would require that an entirely different weak write pull-down transistor be substituted for devices 44, 52, 54 and 56 if "generating" and "applying" were arguably employed with the driver 10 of Vangal. Such a substitution would effectively change the driver 10 of Vangal into another driver rendering the disclosure of Vangal moot.

Therefore, Applicant respectfully submits that the Examiner failed to establish, separately for each of Applicant's base Claims 1, 16 and 20, a *prima facie* case of anticipation with respect to Vangal. Vangal clearly fails to disclose, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, cited *supra*) when considering Applicant's base Claims 1, 16 and 20. In particular, as detailed above, the Examiner failed to show that there is, "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention," as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

In addition to that specifically discussed above with respect to Claims 2-4, the Examiner similarly failed to show that dependent Claims 2-4 and 23 are *prima facie* anticipated by Vangal at least for failing to establish *prima facie* anticipation of respective base Claims 1 and 20. In particular, Claims 2-4 are dependent from and include all of the limitations of base Claim 1 while Claim 23 is dependent from and includes all of the limitations of base Claim 20. Hence, the rejection of Claims 1-4,

16, 20 and 23 under 35 U.S.C. 102(e) over Vangal is unsupported by facts in evidence and should be withdrawn. Reconsideration and withdrawal of the rejection are respectfully requested.

Applicant appreciates the Examiner's allowance of Claim 6-15. Applicant further appreciates the Examiner's acknowledgement of the allowability of Claims 5, 17-19, 21, 22 and 24 if rewritten in independent form. However, in light of Applicant's remarks above, Applicant respectfully submits that Claims 5, 17-19, 21, 22 and 24 are in allowable form, as originally filed. Applicant respectfully declines to rewrite these claims pending the Examiner's consideration of the remarks presented hereinabove for the respective base claims.

In summary, Claims 1-24 are pending. Claims 6-15 were allowed, Claims 1-4, 16, 20 and 23 were rejected, and Claims 5, 17-19, 21, 22 and 24 were objected to. Additionally, Claims 1-5 were objected to due to an informality which is corrected above. It is respectfully requested that Claims 1-5 and 16-24 be allowed along with allowed Claims 6-15, and that the application be passed to issue at an early date.

Should the Examiner's action be other than allowance, the undersigned respectfully requests a telephone call from the Examiner to discuss further consideration that would expedite the prosecution of the application. Furthermore, should the Examiner have any questions regarding the above, please contact the undersigned, J. Michael Johnson, Agent for Applicant, at telephone number (775) 849-3085.

Respectfully submitted,
JOHN WUU ET AL.

By: 
J. Michael Johnson
Attorney/Agent for Applicant(s)
Registration No. 37,856

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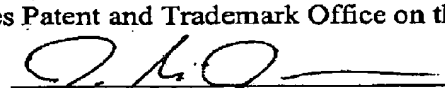
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